

S/N 09/943,393

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Kie Y. Ahn et al.

Serial No.: 09/943,393

Filed: August 30, 2001

Title:

STRUCTURE AND METHOD FOR DUAL GATE OXIDE THICKNESSES

Examiner: Phuc T. Dang

Group Art Unit: 2818

Docket: 303.678US4

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on August 29, 2002, and the references cited therewith.

No claims are amended or cancelled. Claims 41-77 remain pending in this application.

Form 1499

Applicant notes that the Hideo reference as originally submitted by Applicant and listed on the top of sheet 2 of the form 1499 was not initialed as having been considered by the Examiner. Applicant respectfully requests that the Examiner review the Hideo reference and return an initialed form 1499 in the next communication.

§103 Rejection of the Claims

Claims 41-44, 47-51, 55-59, and 62-66 were rejected under 35 USC § 103(a) as being unpatentable over Okazawa (U.S. 4,700,212) in various combinations with Lowrey et al. (U.S. 5,731,238), Hasegawa (U.S. 6,091,109), and Liu et al. (U.S. 5,257,095).

The rejection states that:

Okazawa teaches a circuit on a single substrate, comprising: a logic device (110, Fig. 1), wherein the logic device further includes a transistors with a dielectric layer (42, Fig. 3A) having a first thickness including a top layer (43, Fig. 3A) which exhibits a high resistance to oxidation at high temperatures (1000°C); and a memory device (210, Fig. 1) coupled to the logic device, wherein the memory device further includes a transistor with a dielectric layer having a second thickness greater than the dielectric layer of the first thickness but less than 12 nanometers.

The rejection further states that Lowrey et al. "disclose the dielectric layer of the second thickness is formed entirely of silicon dioxide (SiO_2)."

Lowrey appears to show a first silicon dioxide layer 11 of a first thickness, and a second silicon dioxide layer 41 of a second thickness. However, Lowrey does not show a dielectric layer having a first thickness including **a top layer which exhibits a high resistance to oxidation at high temperatures**. All portions of dielectric layers in Lowrey appear to be fabricated entirely from silicon dioxide.

Okazawa appears to show forming "a thin silicon oxide film 42 and a silicon nitride film 43" (col. 5, lines 37-38), however Okazawa goes on to show removing the silicon nitride film 43 and the silicon oxide film 42 and "newly" forming gate oxide films 29, 39 (col 5, lines 43-45). The resulting dielectric films of Okazawa do not include a dielectric layer having a first thickness including a top layer which exhibits a high resistance to oxidation at high temperatures.

In contrast, Applicant's claim 41 includes a dielectric layer having a first thickness including a top layer which exhibits a high resistance to oxidation at high temperatures. Applicant's independent claims 47, 55, and 62 contain similar language to claim 41. Applicant reserves the right to further distinguish claims 47, 55, and 62 at a later date.

Applicant respectfully submits that the Cavins, Hasegawa, and Liu references fail to cure the deficiencies of Okazawa and Lowrey as discussed above.

Applicant's independent claims, a 35 USC § 103(a) rejection is respectfully requested with references. Reconsideration and withdrawal of the rejection is respectfully requested with respect to Applicant's independent claims 41, 47, 55, and 62. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

Allowable Subject Matter

Claims 67-77 were allowed. Claims 45-46, 52-54, and 60 were objected to as being

Serial Number: 09/943,393

Filing Date: August 30, 2001

Title: STRUCTURE AND METHOD FOR DUAL GATE OXIDE THICKNESSES

dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant acknowledges and thanks the Examiner for allowance of claims 67-77. Further Applicant acknowledges and thanks the Examiner for indication of allowability of claims 45-46, 52-54, and 60 if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant has not amended claims 45-46, 52-54, and 60 to place them in independent form at this time. Pursuant to arguments presented above, Applicant respectfully submits that these claims are in condition for allowance in their present form.

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 09/943,393

Filing Date: August 30, 2001

Title: STRUCTURE AND METHOD FOR DUAL GATE OXIDE THICKNESSES

Page 4
Dkt: 303.678US4

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612- 373-6944) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

KIE Y. AHN ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6944

Date 11-20-02 By [Signature]
David C. Peterson
Reg. No. 47,857

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 20th day of November, 2002.

Name

Amy Moriarty

Signature

[Signature]